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A PC-BASED INSTRUMENTATION BOARD THAT OVERCOMES MANY DRAWBACKS OF TYPICAL COMMERCIAL DATA ACQUISITION SYSTEMS FOR ELECTROPHYSIOLOGICAL RECORDING APPLICATIONS

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Abstract- **The accessibility of adequate instrumentation to conduct fundamental researches for the development of new diagnostic tools and methods in electrophysiology is essential. As such, many researchers develop proprietary instrumentation systems based on commercially available data acquisition boards. These boards are typically not designed for recording electrophysiological signals and as such, they may introduce significant error artifacts such as signal distortions, which in turn may lead to false interpretations. In this paper, we describe a data acquisition board that has the specifications required to adequately record many electrophysiological signals under difficult conditions, as it is often the case in a fundamental research environment. Furthermore, unlike other comparable in-house systems, it enables custom hardware functions to be implemented to support specific requirements encountered in a research environment. The card can also be installed directly in any modern personal computers offering an inexpensive, open, powerful, and very flexible system allowing researchers to easily take advantage of both commercial hardware and software to tailor the final system configuration for their particular needs.**

Keywords **– PCI bus, data acquisition, electrophysiological recording**

I. INTRODUCTION

The PC has become very attractive for scientists and researchers in various fields mainly because of its low price, high computing performance, and the diversity of compatible products available. This selection of products allows researchers to build the required systems by interconnecting various types of commercially available electronic boards. Furthermore, the modern PC not only relies on a very powerful processor for computation but also on a fast interconnection bus well known as the peripheral component interconnect (PCI) bus [1]. More and more manufacturers are building electronic boards including data acquisition boards that can be plugged to the PCI bus [2]. Unfortunately, researchers involved in direct cardiac mapping and/or BSPM could not take advantages of all the resources available in the new PCI-based market. This is due to the fact that typical commercially available data acquisition systems are designed for general-purpose applications and are not suited to deal efficiently with the much higher requirements of applications in electrophysiology such as body surface potential mapping (BSPM) and direct cardiac mapping, just to name a few.

II. MAIN LIMITATIONS OF COMMERCIAL DATA ACQUISITION BOARDS

Typical, commercially available, data acquisition cards are designed to deal with relatively low sensor impedance. This is due in great part to the fact that these cards have an analog multiplexer directly connected at the inputs. Although such a scheme reduces the cost per recording channel, it behaves badly with relatively high-impedance electrodes. One of the problems is electrode polarization due to leakage and/or bias current. The excessive leakage current generated by analog multiplexer increases the input DC offset and hence limits the gain achievable without causing channel saturation. This offset can be reduced through AC coupling but it is well known that AC coupling involves a reduction in CMRR. Furthermore, AC coupling causes undesirable distortion in the low frequency band of the recorded electrophysiological signals. Another problem with systems relying on analog multiplexer at the front-end is the charge coupling effect, extending the total settling time. Because of this increase in the settling time, the scan rate through all electrodes must be reduced significantly unless one can tolerate a loss in resolution due to settling errors. Furthermore, high resolution recording systems such as those relying on 16-bit converters, are more sensitive to such settling errors, and hence, the channel scan rate must be reduced further to maintain the maximum resolution. It then becomes obvious that with high-resolution measurements performed with high impedance electrodes such as the ones encountered in BSPM and cardiac mapping, the scan rate possible in conventional acquisition boards may be reduced to an inadequate value for such studies.

Another source of errors that would typically occur during electrophysiological recordings is caused by the loading effect of the inputs since the input impedance of the data acquisition card is unlikely to be several orders of magnitude greater than the impedance of the electrodes. Another important problem is that most commercial data acquisition cards are not designed to measure very small amplitude signals. First, there is the loss of the dynamic range due to a limited amplification of the input offset generated by relatively large bias and/or leakage current flowing through high impedance electrodes. Secondly, the maximum gain setting itself is often too low to take advantage of the full-scale range (FSR) of the A/D converter because such systems were designed initially to record larger amplitude signals. Another important requirement for BSPM and cardiac mapping is the CMRR. Because of the large impedance involved, external interference can be capacitively and inductively coupled to the very small amplitude electrophysiological signals. Passing differential lines through an analog multiplexer prior to a differential amplifier does not always provide the higher CMRR possible.

III. PROPOSED SYSTEM

A typical system can be made of four of our proposed data acquisition boards (see Fig. 1) plugged into each of the

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Abstract

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four PCI slots available on a standard Pentium-based motherboard. Each board consists of 16 differential input channels for a total of 64 differential input channels per PCI-based system. Each channel has its own FET input instrumentation amplifier providing very high input impedance with low bias current (50 pA maximum). This alone contributes to reduce the input offset amplitude generated by high-impedance electrodes while minimizing any possible loading errors as well as the charge coupling effect. It also improves drastically the CMRR characterized at 110 dB (90 dB at 10 kHz).

Each card has eight 16-bit monolithic successive-approximation A/D converters with 18-bit calibration. Each converter has a maximum sampling rate of 100 kS/s. The scheme implemented allows a maximum sampling rate of 50 kS/s per channel when all channels are sampled and twice this value when recording is performed with half the channels available. This is performed by routing pair of differential channels through an analog duplexer just prior to each A/D converter. The use of an analog duplexer here has minimum effect on the settling time since it is connected to the very low impedance output of the instrumentation amplifiers. The use of eight A/D converters allows over-sampling to be performed. An over-sampling ratio of 50 can be easily achieved assuming the typical 1 kS/s per channel sampling rate requirement for cardiac mapping measurement [3]. Assuming random noises, this over-sampling ratio translates ideally into a possible SNR increase of 17 dB. The converted data are stored in an accumulator, and the sum, with the corresponding number of samples are read simultaneously as a 32-bit word when a particular recording channel is accessed. The average value is simply computed by dividing the accumulator's content by the number of samples. Averaging is a way to increase the SNR in those cases where the frequency spectrum of the noise and the signal overlap. Conventional filtering in such cases does not help since by setting the -3 dB frequency of the filter to reject noise, it will also reject the signal.

Eight converted data words are transmitted simultaneously from the eight A/D converters to a RAM-based Field Programmable Gate Array (FPGA). The primary task of the custom based internal circuit within the FPGA is to convert the digital serial words from the ADCs in parallel forms while providing computer access support, various control functions, decoding, and time-based or event-based interrupt generation.

Among several hardware features available on the card, one that may prove to be very useful to conduct cardiac and body surface mapping is the capability to provide a return path for each input channel while maintaining a very high input impedance. Data acquisition cards generate bias/leakage currents at the inputs. In conventional data acquisition cards, this leakage and/bias current is relatively large. Without a return path provided by bias resistors connected between the input channels and ground, the recorded signals drift due to a charge effect and will typically saturate in a relatively short time. Therefore, bias resistors must be used to eliminate such drift. Unfortunately, adding bias resistors will lower the input impedance to a value equivalent to the value of the bias resistors. Hence, bias resistors should ideally have the highest possible value. Unfortunately, the higher the bias resistor value, the higher the input DC offset due to the leakage/bias currents flowing through the return paths. Such limitation are even more critical when relatively high gain values are being used such as during cardiac and body surface mapping. Hence, in conventional data acquisition systems, the input impedance cannot be set very high, causing significant loading errors when used with conventional electrodes.

With no leakage currents and a maximum bias current per channel of 50 pA for the proposed system, the time at which the signal will saturate without a return path for a GΩ range input impedance will be significantly extended. Because of such low bias current, the bias resistors value can be increased significantly into the MΩ range without causing significant amplifier's output DC offset, even with the maximum possible gain setting of 800 on the present card.

A. Comparison with a Commercial Board

The preceding sections have stressed some of the important characteristics that should be supported by a data acquisition card used for BSPM and cardiac mapping. The goal of this section is to give a feel of the capabilities of such commercial boards to be used as a research tool in these fields.

The PCI-MIO-16XE-50 from National Instruments [4] has been chosen because it is a good example of a PCI-based 16-bit data acquisition board that is targeted to general-purpose applications. The MIO board has a bias current of ±10 nA, a maximum gain of 100, and a FSR of ±10V in bipolar mode. Hence, considering these parameters alone and neglecting all other error artifacts, a 4 MΩ electrode's impedance as encountered in some direct cardiac mapping experiments will generate a maximum output offset of ±4V in the FSR. This alone represents a maximum DC error of ±40% of the FSR. The worst is that we cannot predict such DC error because we do not know the electrode's exact impedance nor do we know the absolute bias current of any particular channel. Worst is the input offset current characterized at ±20 nA. The input offset current is a mismatch between the differential inputs and may contribute significantly to increase the error especially when recording in differential mode. For the Mirada card with a bias current of ±50 pA and a FSR (span) of ±4.5 V in bipolar mode, the maximum DC error with the same gain of 100 in this particular case would be ±0.44% of the FSR.

Another problem is the bias resistor value that would be necessary to avoid baseline drift. If we want to maintain the maximum loading error at 1% for instance, the input impedance needs to be at least 400 MΩ. This alone would generate a DC input offset of 4V for the MIO card, limiting to maximum usable gain to 2. For the Mirada card under the same condition, the maximum input offset generated by the bias resistors would be 20 mV, limiting the maximum usable

gain to 225 which is more adequate when recording small electrophysiological signals.

The previous example may be considered as an extreme situation but is often encountered in direct cardiac mapping studies. Let now consider the BSPM application. The exact impedance of the electrodes placed directly on the body surface to sense the cardiac field is hard to predict and may vary significantly. This is because such impedance will depend on the dermal and epidermal layer of the skin, the layer of electrolytic paste that may be applied to the skin, as well as the electrode itself. The impedance at the sensor level may easily reach the MΩ range if the skin is not well prepared. Mild skin abrasion and cleaning to remove oils can reduce this resistance to under 5000 Ω [5].

Assuming a 5 kΩ electrode's impedance and a 500 kΩ input impedance in order to maintain the loading error below 1%, the maximum input DC offset generated by the bias current would be approximately 5 mV. Assuming that the signal to be recorded has peak amplitude of 1 mV (which is approximately the amplitudes to be expected in this type of study), the maximum input DC offset is already 5 times the signal's amplitude. If the amplitude measurements are done with regard to the baseline and not the ground reference, then such DC offset may not be an issue in this particular case since with a maximum gain of 100, the peak signal would only be 600 mV. To minimize the impact of the A/D quantization error, it is desirable to amplify the signal as close as possible to the full scale (FS) without causing saturation. Unfortunately, with the previous example only 1% of the FS (FSR/2) is occupied by the signal itself reducing the effective resolution to between 8 and 9 bits. With a FSR of ±4.5 Volts, the same signal amplified 100 times on the proposed board will occupy 2.2% of the FS, which is equivalent to an effective resolution of between 9 and 10 bits. This is better than 1 % but ideally we want such value to be as close as possible to 100%.

With a maximum gain of 800 on the actual card, the 1 mV signal becomes 800 mV at the input of the ADC, increasing the percentage of the FS occupied by the signal to 17.8%, which is equivalent to an effective resolution between 12 and 13 bits. This configuration leaves plenty of room for DC offset. With the 500 kΩ input impedance, the worst additional output offset that may add to the 800 mV signal is only 20 mV. One can take advantage of that if amplitude measurements are done with regard to the baseline, by decreasing further the loading error that contributes to attenuate the signal amplitude relative to the baseline. With a gain of 800, the maximum input DC offset that can be tolerated is 4.625 mV, limiting the maximum bias resistors to a value as high as 92.5 MΩ neglecting all other error artifacts.

IV. Hardware Reconfiguration

The acquisition cards used for experimentation in electrophysiology are most often a commercial system adapted to fulfill the requirement of the experiment. Although changes in software may be adequate and sufficient to fulfill many requirements, some functions can only be performed in hardware. Furthermore, many functions performed in software, especially repetitive tasks, can execute orders of magnitude faster when implemented in hardware.

Providing a data acquisition card that allows user-defined functions to be embedded in hardware can be a valuable and powerful tool for many experimentalists. The basic theory and a description of an example of an implementation are provided in the following sections

The FPGA used in this particular experimental system is a XC4013E [6] containing 13,000 usable gates. The design of the acquisition card allows it to be plugged onto a high performance PCI bus available in all modern personal computers (PC). When the computer is first powered up, a default hardware configuration file or bitstream is downloaded automatically onto a RAM-based FPGA resident on the data acquisition board. The default reconfigurable hardware implements the basic functions required by the card and by most applications. Although several functions are optional at this stage and could be implemented at a later time through a subsequent reconfiguration process, two of these functions are mandatory in the initial reconfigurable implementation to make subsequent hardware reconfigurations possible.

The first mandatory function is the communication interface with the PCI controller [7]. The hardware resources on the data acquisition card are accessed by software through the PCI bus and the PCI controller embedded on the card. Once an access is detected, the communication interface embedded in the FPGA is flagged and several steps are initiated to transfers data using a handshake protocol between the PCI controller and the FPGA. The second mandatory embedded functions is the reconfiguration control block that will allow writing the new hardware reconfiguration file received through the communication interface to the configuration memory and to re-initiate a new reconfiguration phase upon completion of the loading process. During the reconfiguration process, the EPROM that contained the initial default bitstream is disabled and the new bitstream is downloaded from the configuration memory. The reconfiguration time may vary slightly but on the present implementation, approximately 30 ms is required to implement a new semi-custom hardware system. Prior to downloading, the bitstream files could be located anywhere including an attached hard drive, or transferred from other locations through the Internet.

A. Hardware Support

The FPGA is the largest integrated circuit (IC) and it is located on the right and next to the PCI controller. An EPROM next to the FPGA contains the default reconfigurable hardware file, which is downloaded during power-up. The configuration memory is implemented by two static RAM (SRAM) components. The FPGA is connected to eight 16-bit A/D converters running at 100 kS/s each. The converters support 16 recording channels where the analog signals are amplified by 16 FET-input (high input impedance) instrumentation amplifiers. The remaining functions required

for reconfiguration, data transfer, interfaces with the A/D converters, and potential reconfigurable computing functions are all implemented in the FPGA.

B. Methodology

The hardware functions can be described using schematic entry methodology, finite states machine (FSM), or using a hardware description language (HDL). The two main HDL in widespread use today are VHDL and Verilog. For portability and productivity, we describe the hardware functions by using HDL instead of schematic entry. We use HDL to model the digital functions at many levels of abstraction, ranging from the algorithm level to the gate level. Timing specifications can also be modeled in the same description. Very complex functions can also be adequately modeled using a hierarchical approach. We also describe such functions using various modeling styles namely, structural, data-flow, behavioral, and mixed [8].

To accelerate the description of complex hardware functions, we are developing various cores. Cores are like hardware objects (components) that can be interconnected to build the required functions. Cores can be provided as soft, firm, and/or hard cores. Soft cores do not guarantee any timing specifications but are versatile and highly portable whereas hard cores guarantee timing specifications but are technology dependent and inflexible. Firm cores are a trade-off between soft and hard cores.

Once a design has been described using a HDL, it is first synthesized and a functional simulation is performed. Logic synthesis is the process of turning a language description into gates. Once both synthesis and functional simulation are completed, the logic is partitioned accordingly to the size and architecture of the configurable logic blocks (CLB) in the FPGA. After the partitioning phase, a place-and-route process is performed to interconnect the CLBs accordingly to the FPGA's physical structure. A constraint file indicating the locations of the FPGA's physical pin has been created to guide the place-and-route process. The constraint file ensures that both the physical layout of the board and the reconfigurable implementation, interconnect in a proper way. The same constraint file can be used for all reconfigurable designs provided that they are intended for the same type of electrophysiological recording board i.e. with the same physical layout. When the partition-place-and-route (PPR) phase is completed, back annotation and timing simulation are performed to validate the design against timing violations and performance goals. To help in achieving the performance goals for very complex designs, floor planning is also available as an additional phase in the development cycle. The resulting circuit is converted as a bitstream file that can be downloaded into the electrophysiological recording board.

The density of the actual FPGA can support several functions simultaneously but is insufficient for many more complex reconfigurable computing functions. Complex system-on-a-chip (SOC) will be supported by FPGA in a very near future. As the density of FPGA increases drastically in parallel with better hardware/software co-design methodologies and the increase availability of intellectual property (IP) cores, complex systems including sophisticated reconfigurable signal processing functions will be available and their implementation feasible in systems similar to the one described in this paper.

V. SUMMARY

Commercial general-purpose acquisition boards are far from ideal for electrophysiological recording, although they can be used in good experimental conditions and if the user is well aware of the limitations and the errors introduced when measuring the signals. A modified card can make a huge difference in the quality of the recorded signals while being better designed to deal with larger impedance electrodes. The board briefly described in this paper is a low cost PC-based alternative for cardiac mapping and BSPM, providing more trustable data that will likely minimize uncertainties than traditional PC-based data acquisition products when developing the torso model.

The present system also allows custom digital functions to be described and embedded onto the data acquisition card. With such approach, a data acquisition card can be custom made within some constraints at minimum cost and with very short development time. Furthermore, several subsequent hardware modifications and/or improvement can be made without replacing the physical implementation. Several cards can also be plugged onto the same personal computers to increase the capability of the system.

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